REMARKS

Claims 1-30 stand rejected. In addition, the specification and the claims are objected to. Claim 16 is cancelled herein because the features of previously present claim 16 are amended into independent claim 15. Thus, claims 1-15 and 17-30 are all the claims presently pending in the application. Applicants respectfully traverse the rejection of these claims based on the following discussion.

I. The Objections

A substitute specification is provided in order to overcome the objections to the specification. Additionally, the claims are amended herein in order to overcome the objections to the claims. In view of the foregoing, the Applicants respectfully request that the objections to the specification and claims be withdrawn.

II. The 35 U.S.C. § 112 Rejection

Claims 3, 7, 12, 17, 19, 26, and 22 stand rejected under 35 U.S.C. §112, second paragraph. The claims have been amended, above, to overcome this rejection. In view of the foregoing, the Examiner the use respectfully requested to reconsider and withdraw this rejection.

III. The Prior Art Rejections

Claims 1-28 and 30 stand rejected under 35 U.S.C. §102(e) as being anticipated by Jacobson (U.S. Patent No. 7,073,110), hereinafter referred to as Jacobson. Claim 29 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of Nadeau-Dostie et al. (U.S. Patent No. 6,829,730), hereinafter referred to as Nadeau-Dostie. Applicants

respectfully traverse these rejections based on the following discussion.

Jacobson discloses a flexible architecture for extending an instruction set. In one embodiment, in a programmable instruction register and logic 304 an instruction can be selected from a memory store 308, which stores user-defined instruction that can be used to extend an existing instruction set, and decoded by a decoder 310. The instruction can subsequently be shifted into an instruction register 349 where it can be executed (see Abstract, Figures 3a-b, and col. 7, lines 21-col. 8, line 48). Alternatively, a length of an existing instruction register (382) can be programmable appended to effectively increase the length of the resister. A plurality of serially arranged bit registers (376, 378, 380) can be connected in series with the existing instruction register. By selecting an outer on of the serially arranged bit registers, the length of the existing instruction register can be extended (see Abstract, Figure 3c and col. 8, line 49- col. 9, line 51). Thus, as explained in col. 9, lines 11-30, each of the bit registers 376, 378, 380 incrementally extend the length x of the fixed bit register 382 by one bit. For example, selection of bit register 376 will extend the length x of the fixed bit register 382 by 1 bit (providing a total length of x+1bit), selection of bit register 378 will extend the length x of the fixed bit register 382 by 2 bits (providing a total length of x+2bits) and so on until the selection of bit register 380 which will extend the length the fixed bit registers 380 by N bits (providing a total length of x+Nbits). To allow for selection of a particular bit register, each bit register is coupled to a corresponding selector which in turn is coupled to a programmable bit select register. Each of the programmable bit select registers can be programmed to enable its corresponding selector to select its corresponding bit register.

Contrarily, as disclosed in paragraphs [0021-0023] and illustrated in Figure 1, in the present invention the chip level TAB comprises a flexible length instruction registers that comprises a plurality of instruction register segments and additional bit segments. The instruction register segments comprise a first instruction register segment that has the same length (E.g., 4 bits) as the shortest embedded TAP instruction register and at least two other instruction register segments that have lengths equal to a difference between a previous shorter embedded TAP instruction register and a next longer embedded TAP instruction register (e.g., a second register segment that has a length equal to the difference between the shortest embedded TAP instruction register and a next longer embedded TAP instruction register). The combined length of the instruction register segments is equal to a longest embedded TAP instruction register and additional bit segments. Thus, with the additional bit segments the flexible length instruction register is longer than the longest embedded TAP instruction register. The additional bit segments are adapted to choose effective length of the flexible length instruction which is equal to a combined length of the first instruction register segment and any selected other instruction register segments so as to match the length of a particular one of the embedded TAP instruction registers.

A. Rejection Of Amended Independent Claim 1 Based On Jacobson

The Applicants submit that Jacobson does not teach or suggest the following feature of amended independent claim 1: "wherein said flexible length instruction register comprises a plurality of instruction register segments, wherein at least two of said instruction register segments comprise multiple bits".

As discussed above, only the fixed length bit register 382 of Jacobson with a length of x has multiple bits. The bit registers 376, 378, etc. each comprise single bits that are added incrementally to the fixed length bit register to increase its length by one additional bit (e.g., to provided combined lengths of x+1, x+2, etc.). Thus, Jacobson does not teach a plurality of instruction register segments, wherein at least two of said instruction register segments comprise multiple bits.

B. Rejection Of Amended Independent Claim 10 Based On Jacobson

The Applicants submit that Jacobson does not teach or suggest the following features of amended independent claim 10: (1) "a plurality of instruction register segments at least two of which comprise multiple bits, at least two of said instruction register segments comprise multiple bits"; and (2) "wherein said plurality of instruction register segments comprise: a first instruction register segment having a same length as a shortest embedded TAP instruction register and a second instruction register segment having a length equal to a difference between said shortest embedded TAP instruction register and a next longer embedded TAP instruction register."

As discussed above, only the fixed length bit register 382 of Jacobson with a length of x has multiple bits. No where in Jacobson is it disclosed that this length x is a same length as that of the shortest embedded TAP instruction register. Additionally, the bit registers 376, 378, etc. each comprise single bits that are added incrementally to the fixed length bit register to increase its length by one additional bit (e.g., to provided combined lengths of x+1, x+2, etc.). No wherein Jacobson does it disclose that a second instruction register segment (e.g., 376) has a length equal to the difference between the length of the shortest embedded TAP instruction register and a next longer embedded TAP instruction register." Thus, Jacobson does not teach a plurality of instruction register segments of which at least two comprise multiple bits, nor does it teach what the lengths of those segments correspond to (other than 1).

C. Rejection Of Amended Independent Claim 15 Based On Jacobson

The Applicants submit that Jacobson does not teach or suggest the following features of amended independent claim 15: (1) "wherein said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded

TAP instruction register and additional bit segments such that said flexible length instruction register is longer than said longest embedded TAP instruction register"; (2) "wherein said plurality of instruction register segments comprise a first instruction register segment comprising": (a) "multiple bits and having a same length as a shortest embedded TAP instruction register"and (b) "at least two other instruction register segments having lengths equal to a difference between a previous shorter embedded TAP instruction register and a next longer embedded TAP instruction register"; (3) "wherein at least one of said at least two other instruction register segments comprises multiple bits."

As discussed above, only the fixed length bit register 382 of Jacobson with a length of x has multiple bits. No where in Jacobson is it disclosed that this length x is a same length as that of the shortest embedded TAP instruction register. Additionally, the bit registers 376, 378, etc. each comprise single bits that are added incrementally to the fixed length bit register to increase its length by one additional bit (e.g., to provided combined lengths of x+1, x+2, etc.). Jacobson discloses that the combined length of the fixed length bit register and all of the other bit registers is x+Nbits, but no where in Jacobson does it disclose what this length x-Nbits corresponds to, much less that x+Nbits is longer than the longest embedded TAP instruction registers. Additionally, while Jacobson does disclose bit registers 376, 378, 380 in addition to the fixed length bit registers 382, it only discloses that each of these bit registers has one bit. It does not disclose that they have lengths greater than one or particularly lengths equal to a difference between a previous shorter embedded TAP instruction register and a next longer embedded TAP instruction register or that at least two of them comprise multiple bits.

D. **Rejection Of Amended Independent Claim 22 Based On Jacobson**

The Applicants submit that Jacobson does not teach or suggest the following features of amended independent claim 22: (1) "wherein said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction register is longer than the longest embedded TAP instruction register"; and (2) "wherein said additional bit segments are adapted to choose an effective length of said flexible length instruction register."

As discussed above, the bit registers 376, 378, etc. of Jacobson each comprise single bits that are added incrementally to the fixed length bit register to increase its length by one additional bit (e.g., to provided combined lengths of x+1, x+2, etc.). Jacobson discloses that the combined length of the fixed length bit register and all of the other bit registers is x+Nbits, but no where in Jacobson does it disclose what this length x-Nbits corresponds to, much less that x+Nbits is longer than the longest embedded TAP instruction registers. Additionally, while Jacobson does disclose bit registers 376, 378, 380 in addition to the fixed length bit registers 382, it only discloses that these bit registers are adapted to be loaded with TDIs, it does not disclose that any of the bits in the programmable bit register are adapted to choose an effective length. That is, col. 9, lines 11-51 of Jacobson discusses how the programmable bit registers of 304c operate. Specifically, a specific programmable bit select register can be programmed to enable a corresponding selector which in turn selects its corresponding bit register (e.g., bit select register 368 can be programmed to enable selector 374 and thereby to select outer bit register 380), which in turn results in the selection of all bit registers from the fixed bit register 382 to the outer

bit register 380. No wherein in Jacobson does it disclose additional bit segments that are adapted to choose an effective length of the flexible length instruction register.

Therefore, amended independent claims 1, 10, 15 and 22 are patentable over Jacobson. Further, dependent claims 2-9, 11-14, 17-21 and 23-30 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

IV. Formal Matters and Conclusion

A Substitute Specification is being submitted herewith to overcome the objections to the specification. The Examiner is, thus, respectfully requested to withdraw the objection to the specification.

Additionally, the claims have been amended, above, to overcome the objections to and rejections of the claims. In view of the foregoing, Applicants submit that claims 1-15 and 17-30, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to

discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 10/23/06

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SUBSTITUTE SPECIFICATION
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ACCESS METHOD FOR EMBEDDED JTAG TAP CONTROLLER INSTRUCTION REGISTERS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention generally relates to an integrated circuit chip structure that has a chip level test access port (TAP) controller and more particularly to a chip that also includes a plurality of embedded TAPs connected to the chip level TAP. Because the embedded TAPs have instruction register (IR) lengths that differ from the chip level TAP IR, and the embedded TAP IR lengths may differ from each other, the chip level TAP includes a flexible length instruction register architecture designed to accommodate the different length instruction registers of the embedded TAPs while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP.

Description of the Related Art

[0002] As explained in U.S. Patent 6,334,198 (incorporated herein are reference), the electronics industry continues to rely upon advances in semiconductor technology to realize higher-functioning devices in more compact areas. For many applications, realizing higher-functioning devices requires integrating a large number of electronic devices into a single silicon wafer. As the number of electronic devices per given area of the silicon wafer increases, the manufacturing process becomes more difficult.

[0003] A wide variety of techniques have been used in IC devices to ensure that, once they are manufactured, they operate fully in compliance with their intended design and

implementation specifications. Many of the more complex IC designs include circuits that permit in-circuit testing via the IC access pins. The IEEE 1149.1 JTAG recommendation, for example, provides a test circuit architecture for use inside such ICs. This architecture includes a test access port (TAP) controller coupled to the IC pins for providing access to and for controlling various standard features designed into such ICs. Some of these features are internal scan, boundary scan, built-in test, and emulation.

[0004] The JTAG recommendation was developed with the understanding that such IC designs would be using only one TAP controller. Sometime after the TAPs, initial development, however, many IC's were designed with multiple "core" circuits, such as multiple CPUs, with each core circuit including its own TAP controller. Typically, separate IC pins are used to select one of the TAP controllers for testing and/or debugging the IC. This is problematic, however, in IC applications that require an increasing number of core circuits without increasing the circuit area of the IC and/or the number of IC pins.

[0005] ASIC (application specific integrated circuit) devices, usually contain a single JTAG TAP controller for access and control of board level tests of I/O continuity. Access to user defined functions can also be supported using the chip level TAP controller and private instruction definitions. When integrating large intellectual property (IP) blocks into today's ASICs there is the possibility that such IP will have embedded JTAG access through a self contained TAP controller. Access methods for embedded TAP functions are not covered in the IEEE 1149.1 JTAG specification. Methods have evolved, independent of the IEEE 1149.1 specification, that enable access to embedded TAP controllers through the use of various implementations of compliance enable logic and private instruction definitions in the ASICs chip level TAP controller. These methods strive to maintain IEEE 1149.1 JTAG compliance; however, one limitation of these existing methods is the inability to shift out (or read) differing length embedded TAP instruction registers with a single chip level instruction register length definition as is required for IEEE 1149.1 compliance.

[0006] This invention described below allows IEEE 1149.1 compliant shifting out (reading) of embedded JTAG TAP controller instruction register (IR) contents, contained in IP blocks on ASIC chips, while using a constant length chip level instruction register definition for

all IR accesses through the chip level TAP.

SUMMARY OF THE INVENTION

[0007] This disclosure presents an integrated circuit chip structure that has a chip level test access port (TAP) controller and a plurality of embedded TAPs connected to the chip level TAP. Because the embedded TAPs have instruction register lengths that differ from the chip level TAP IR, and the embedded TAP IR lengths may differ from each other, the chip level TAP includes a flexible length instruction register architecture designed to accommodate the different length instruction registers of the embedded TAPs, while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. Further, the invention includes selection logic adapted to actively connect only a single embedded TAP to the chip level TAP at a time.

[0008] This chip-level flexible length instruction register length is longer than the longest embedded TAP instruction register, and the additional bits that make the flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of the flexible length instruction register.

[0009] The inventive flexible length instruction register comprises of several segments of register bits, including a plurality of multiplexers used to selectively concatenate or bypass the register segments with the selected embedded TAP instruction register bits, maintaining a constant length chip-level TAP instruction register. The length of the register segments are, for example in one embodiment, a first instruction register segment having the same length as the shortest embedded TAP instruction register, and a second instruction register segment having a length equal to the difference between the shortest embedded TAP instruction register and a larger embedded TAP instruction register. More generally, the flexible length instruction register comprises additional instruction registers segments having incremental lengths equal to the difference between the previous shorter embedded TAP instruction register and the next

largest embedded TAP instruction register.

[0010] The invention includes a plurality of multiplexors connected to the additional instruction registers segments, wherein the multiplexors are adapted to selectively include incremental ones of the additional instruction registers segments to incrementally match the difference in length of longer embedded TAP instruction registers and the chip-level TAP instruction register. Thus, the active length of the flexible length instruction register comprises the selected embedded TAP instruction register bits combined with selected ones of the additional instruction registers segments of the chip-level TAP instruction register.

[0011] One benefit of the invention is that the flexible length instruction register appears as a fixed length instruction register to users connecting to the chip level TAP. Therefore, the invention allows IEEE 1149.1 compliant access (reading) of embedded JTAG TAP controller instruction register (IR) contents, contained in IP blocks on ASIC chips, while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. More specifically, the invention allows positional bit replacement of the chip level TAP IR data with embedded TAP IR data. The new architecture allows for a single IR length definition to represent and access all embedded and chip level TAP instruction registers.

These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0013] Figure 1 is a conceptual diagram of the chip level and embedded TAPs used with the inventive structure;

[0014] Figure 2 is a schematic diagram of different length instruction registers included within the chip level and embedded TAPs;

[0015] Figure 3 is a schematic diagram of the chip level and embedded TAPs used with the inventive structure; and

[0016] Figure 4 is a schematic diagram of the chip level and embedded TAPs used with the inventive structure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0017] The present invention and the various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0018] Figure 1 illustrates a first embodiment of the inventive integrated circuit chip structure. As shown in Figure 1, the chip 100 (which can be, for example an ASIC) includes a chip level test access port (TAP) controller 102 and a plurality of embedded TAPs 104-110 connected to the chip level TAP. A user 150 will access the data within the embedded TAPs 104-110 through the chip level TAP controller 102. Note that the length of the instruction registers 112-118 within each of the embedded TAPs is inconsistent. For example, instruction register 112 is four bits long, instruction registers 114 and 116 are six bits long, and instruction register 118 is ten bits long.

[0019] Because the embedded TAPs have different length instruction registers, the chip level TAP includes a flexible length instruction register architecture 120 adapted to accommodate the different length instruction registers 112-118 of the embedded TAPs 104-110. Further, the invention includes selection logic 130 adapted to actively connect only a single embedded TAP to the chip level TAP 102 at a time.

[0020] The inventive flexible length instruction register 120 has, for example in one embodiment, a first instruction register segment 122 having the same length (e.g., 4 bits) as the shortest embedded TAP instruction register 112, and an additional instruction registers segment (e.g., 2 bit register segment 124) that has an incremental lengths equal to the difference between the previous shorter four bit embedded TAP instruction register 112 and the next largest six bit embedded TAP instruction registers 114, 116, and a third additional instruction register segment (e.g. 4 bit register segment 126) that has an incremental length equal to the difference between the sum of the previous register segments 124 and 122 and the length of embedded TAP instruction register 118. Therefore, when connected to embedded register 118, the invention only actively utilizes the last instruction register segment 128 to shift out (read) the data from the embedded register 118. To the contrary, the invention will utilize both the last and next to last instruction registers segments 128 and 126 to make the flexible length instruction register 120 six bits long, when shifting out data from the six bit embedded registers 114, 116. Similarly, when reading out data from the four bit embedded TAP instruction register 112, the flexible length instruction register 120 will become eight bits in length by engaging the last three instruction register segments 124, 126 and 128. When accessing the chip level TAP, the flexible length instruction register 120 will become a 12 bit instruction register by engaging all four instruction register segments 122-128.

[0021] The flexible length instruction register 120 is longer than the longest embedded TAP instruction register. More specifically, the flexible length instruction register 120 has a total of 12 bits divided into separate registers 122-128. The additional bits 128 that make the flexible length instruction register longer than the longest embedded TAP instruction register (e.g., 10 bit register 118) comprises bits 128 that are adapted to choose the effective (active) length of the flexible length instruction register. The selection logic 130 uses the information

within the additional bits 128 to identify which embedded TAP will be connected to the chip level TAP 120 and which corresponding registers segments 122-126 will be utilized within the flexible length instruction register 120 to access (shift out) the data from the selected embedded TAP.

[0022] The integrated circuit chip 100 shown in Figure 1 includes four embedded TAPs 104-110 and three different length instruction registers; however, as would be understood by one ordinarily skilled in the art in light of this disclosure, any number of embedded TAPs and any number of different length instruction registers could be accommodated with the invention, and the invention is not limited to the specific examples used herein. Further, the selection logic 130 could comprise a wide variety of logic devices as would be understood by one ordinarily skilled in the art. For example, selection logic 130 could include a plurality of multiplexors connected to the instruction registers segments 122-126, wherein the multiplexors could selectively include incremental ones of the additional instruction registers segments to incrementally match the difference in length of the embedded TAPs instruction registers and the chip level TAP IR length definition. Thus, the active length of the flexible length instruction register 120 comprises the length of the additional bits 128 combined with selected ones of the additional instruction registers segments 122-126.

[0023] Figures 2 and 3 illustrate a more specific schematic circuit diagram of the invention as it would apply to an integrated circuit chip that included two embedded TAPs 300, 302. More specifically, Figure 2 illustrates the instruction shift registers 200-204 that are found within the first embedded TAP 300, second embedded TAP 302, and the chip level TAP 304, respectively, that are shown in Figure 3.

[0024] A given embedded TAP instruction register 200, 202 "maps" onto the chip-level instruction register 310-314 starting at the most significant bit (MSB) such as bit 9 of the IR definition and proceeding downwards as shown in Figure 2. Figure 2 illustrates two embedded TAP IRs 200, 202 that are 5 and 8 bits in length, respectively, for embedded TAP #1 300 and embedded TAP #2 302. As shown in Figure 3, the chip-level TAP IR is 10 bits in length (L=K+D) where K is equal to the total of the individual shift registers 310, 312 and D is equal to the number of additional control bits 314. More specifically, the chip-level TAP instruction

register is designed with a length L = K+D, where K>= (length of longest instruction register, or string of instruction registers if serially connected, among TAPS in embedded IP blocks) and 2D >N, where N= (# of TAPs in embedded IP blocks). The D low-order bits of the instruction register will be used for selecting access to the TAP within one of the N IP blocks or for selecting a chip-level instruction.

[0025] Figure 3 shows that when a TAP controller of embedded IP blocks is accessed by the decoded D low-order bits 314 of the instruction register (bits[1:0]), and the SHIFT-IR state is entered by the chip-level TAP controller 304, the chip-level TAP IR is instructed (by the TAP logic unit 322) to connect the embedded TAP test data output (TDO) signal in place of the instruction register bit corresponding to the length of the chip-level IR, less the length of the selected embedded TAP IR. For embedded TAP #1, as defined above, this is bit 5 (10-5), IR5 shown in Figure 2; for embedded TAP #2, this is bit 2 (10-8), IR2 shown in Figure 2.

[0026] With respect to the additional structure shown in Figure 3, the TAP logic unit 322 can receive a number of different inputs including a test clock signal (TCK), a test data input (TDI), the low order bits (IR1, IR0) that identify which, if any, embedded TAP controller will be accessed, a test mode select signal (TMS) that controls test operations, and a test reset signal (TRST). Using these inputs, the TAP logic controller 322 controls AND gates 318, which in turn control multiplexors 316 to selectively utilize none, one, or both of the shift register 310, 312. The same control signals that are sent to AND gates 318 are also provided to the OR gates 320 to enable or disable the embedded TAP controllers 300, 302 so that no more than one of the embedded TAP controllers is providing data to the chip-level TAP at a time.

[0027] The structure shown in Figure 3 allows the TAP controller, in the selected embedded IP block, to track synchronously, state for state, with the chip-level TAP controller logical state. Since the selected embedded TAP controller and the chip-level TAP controller will be running synchronously, when a SHIFT-IR state is entered by the chip-level TAP logic 322, it is also entered in the selected embedded TAP controller. Under these conditions the IR shift out of the chip-level TAP controller will match the "mapped" definition shown in Figure 2. As shown in Figure 3, with embedded TAP #1 300 selected, the first 5 bits will come from the chip-level TAP IR segments 312, 314 and the last 5 bits will come from the embedded TAP IR 300

rather then from register segment 310. In a similar manner, if TAP #2 302 is being accessed, its eight bits of data will be preceded by the two bits from the chip-level TAP instruction register segment 314.

[0028] While the invention has been described in terms of selecting between two TAPs of differing instruction register lengths, those skilled in the art will recognize that the invention also applies equally to a single embedded tap or to multiple serial strings of embedded TAPs, as shown in Figure 4. The length of the instruction register of TAP string #[[1]] 2 is the sum of the lengths of instruction registers in embedded TAPs #1a, [[–]] 1b...1n, 400-402.

[0029] Therefore, as shown above, one benefit of the invention is that the flexible length instruction register appears as a fixed length instruction register to users connecting to the chip level TAP. Therefore, the invention allows IEEE 1149.1 compliant access (reading) of embedded JTAG TAP controller instruction register (IR) contents, contained in IP blocks on ASIC chips, while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. More specifically, the invention allows positional bit replacement of the chip level TAP IR data with embedded TAP IR data. The inventive architecture allows for a single IR length definition to represent and access all embedded and chip level TAP instruction registers.

[0030] In the invention, there is no need for chip-level Compliance-Enable (CE) pins (the invention maintains compliance to the Standard while solving a problem not addressed by the Standard). The invention does not add to board-test complexity (control/access to CE pins). Further, in the invention, no special treatment is needed at test time or during functional operation. The invention does not require multiple BSDL files to account for different instruction register lengths. The invention eliminates need for extra I/O dedicated to test.

[0031] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. An integrated circuit structure comprising:

a chip level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip-level TAP instruction register, and

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs.

2. The integrated circuit structure in claim 1, wherein said flexible length instruction register is longer than the longest embedded TAP instruction register.

3. The integrated circuit structure in claim 2, wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active segments of said flexible length instruction register.

4. The integrated circuit structure in claim 1, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded tapped instruction register.

5. The integrated circuit structure in claim 1, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

additional instruction registers segments having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded TAP instruction register.

6. The integrated circuit structure in claim 5, further comprising a plurality of multiplexors connected to said additional instruction register segments, wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction register segments to incrementally match the difference in length between longer embedded TAPs instruction registers and the chip-level TAP instruction register length.

7. The integrated circuit structure in claim 5, wherein the active length of said flexible length instruction register comprises the selected ones of said additional instruction registers segments.

8. The integrated circuit structure in claim 1, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP.

9. The integrated circuit structure in claim 1, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

10. An integrated circuit structure comprising:

a chip level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other,

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs, and

wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded tapped instruction register.

11. The integrated circuit structure in claim 10, wherein said flexible length instruction register is longer than the longest embedded TAP instruction register.

12. The integrated circuit structure in claim 11, wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register.

13. The integrated circuit structure in claim 10, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP.

14. The integrated circuit structure in claim 10, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

15. An integrated circuit structure comprising:

a chip level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may

differ from each other,

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs, and

wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

additional instruction register segments having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded tapped instruction register.

16. The integrated circuit structure in claim 15, wherein said flexible length instruction register is longer than the longest embedded TAP instruction register.

17. The integrated circuit structure in claim 16, wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register.

18. The integrated circuit structure in claim 15, further comprising a plurality of multiplexors connected to said additional instruction registers segments, wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction registers segments to incrementally match the difference in length between longer embedded TAPs instruction registers and the chip-level TAP instruction register length.

19. The integrated circuit structure in claim 15, wherein the active length of said flexible length instruction register comprises the selected ones of said additional instruction register segments.

20. The integrated circuit structure in claim 15, wherein said flexible length instruction

register appears as a fixed length instruction register to users connecting to said chip level TAP.

21. The integrated circuit structure in claim 15, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

22. An integrated circuit structure comprising:

a chip level test access port (TAP) controller; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other,

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs,

wherein said flexible length instruction register is longer than the longest embedded TAP instruction register, and

wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register.

23. The integrated circuit structure in claim 22, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded tapped instruction register.

24. The integrated circuit structure in claim 22, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP

instruction register; and

additional instruction registers segments having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded tapped instruction register.

25. The integrated circuit structure in claim 24, further comprising a plurality of multiplexors connected to said additional instruction registers, wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction registers segments to incrementally match the length of longer embedded TAPs instruction registers.

26. The integrated circuit structure in claim 24, wherein the active length of said flexible length instruction register comprises the selected ones of said additional instruction register segments.

27. The integrated circuit structure in claim 22, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP.

28. The integrated circuit structure in claim 22, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

29. The integrated circuit structure in claim 22, wherein said embedded TAPs comprise serially connected TAPs.

30. The integrated circuit structure in claim 22, wherein the number of said embedded TAPs is unlimited.

ACCESS METHOD FOR EMBEDDED JTAG TAP CONTROLLER INSTRUCTION REGISTERS

ABSTRACT

Disclosed is an integrated circuit chip structure that has a chip level test access port (TAP) controller and a plurality of embedded TAPs connected to the chip level TAP. Because the embedded TAPs have lengths that differ from the chip level TAP IR, and the embedded TAP IR lengths may differ from each, the chip level TAP includes a flexible length instruction register architecture adapted to accommodate the different length instruction registers of the embedded TAPs while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. Further, the invention includes selection logic adapted to actively connect only a single embedded TAP to the chip level TAP at a time.